

Low Noise Preamplifier ASIC for the PANDA Experiment

Holger Flemming^a and Peter Wieczorek^{a*}

*^aGSI Helmholtzzentrum für Schwerionenforschung GmbH
Planckstrasse 1, Darmstadt
E-mail: p.wieczorek@gsi.de*

ABSTRACT:

For the electromagnetic calorimeter of the PANDA detector a preamplifier ASIC named APFEL (ASIC for Panda Front-end Electronics) has been developed at GSI. It is optimized for the readout of large area avalanche photodiodes (LAAPD) with a capacitance of 300 pF and an event rate of 350 kHz. The ASIC has two equivalent analog channels each consisting of a charge sensitive amplifier, a shaper stage and differential output drivers. For operating the ASIC in a wide temperature range programmable voltage references are implemented on chip.

KEYWORDS: charge sensitive preamplifier ASIC; avalanche photodiode; PANDA experiment.

*Corresponding author.



Contents

1. Introduction	1
2. PANDA Experiment	1
2.1 Electromagnetic Calorimeter	2
3. Readout Electronics	3
3.1 Charge Sensitive Preamplifier	3
3.2 The Shaper and Output Stage	4
3.3 Digital Part	5
4. Measured Results	6
5. Summary	7

1. Introduction

A During the next years in the region of Darmstadt (Germany) a new accelerator facility will be build which will provided high intensity heavy ion beam and colled antiprotons for various experimental use.

PANDA (antiproton annihilation at Darmstadt) is a next generation hadron physics detector planned to be operated at this facility for antiproton and ion research (FAIR). The PANDA collaboration intends to do basic research on various topics around the weak and strong forces, exotic states of matter and the structure of hadrons.

After a short overview of the PANDA Experiment and the electromagnetic calorimeter in section 2 this paper describes the integrated preamplifier and shaper for the calorimeter readout. At the end performance measurements are presented and short summary is given.

2. PANDA Experiment

The future detector will be able to provide precise trajectory reconstruction, energy, momentum measurements and very efficient identification of charged particles.

The Detector consisting of the target, the vertex detector MVD, the straw tube tracker STT, electromagnetic calorimeter EMC, cherenkov detectors DIRC and RICH, the drift chambers MDC and the myon detector. As magnets are foreseen the solenoid and the dipole [1]. The proposed detector shown in figure 1 is subdivided into the target spectrometer consisting of a solenoid around the interaction region and a forward spectrometer based on a dipole magnet to momentum-analyze the forward-going particles The combination of two spectrometers allows a full angular coverage [1].

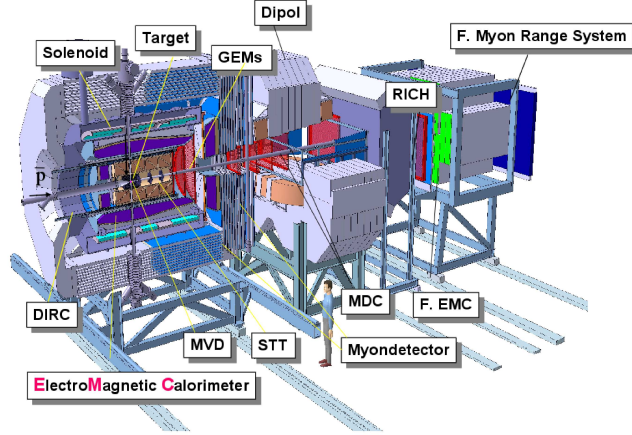


Figure 1. Overview of the PANDA detector.

For energy measurements of photons, electrons and positrons an electromagnetic calorimeter is foreseen. The calorimeter is described into the barrel part, the forward and backend endcap. The barrel part consists of 11000 lead tungstate crystals. The next section will describe the readout of these crystals.

2.1 Electromagnetic Calorimeter

Each crystal of barrel part of the electromagnetic calorimeter is read out by 2 avalanche photo diodes (APD) with an active area of about 1 cm^2 and a detector capacitance of 300 pF. For readout an integrated preamplifier and shaper was developed.

ENC:	< 1	fC
Max. input charge:	> 6	pC
Detector capacitance:	300	pF
Event rate per channel:	up to 350	kHz
Operation temperature:	- 20	$^{\circ}\text{C}$
Power consumption:	< 60	mW/channel
Number of channels:	$\approx 22\,000$	1

Table 1. Summary of PANDA - EMC readout requirements.

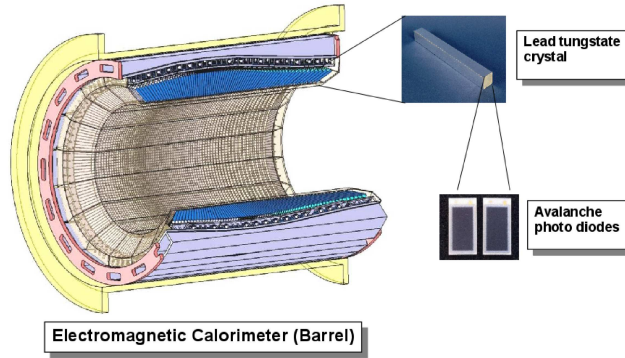


Figure 2. The electromagnetic calorimeter (EMC) of the PANDA detector. As scintillator material lead tungstate will be used. Each lead tungstate crystal will be read out with two avalanche photo diodes (APDs).

3. Readout Electronics

Table 1 shows the requirements for the PANDA electromagnetic calorimeter readout electronics. This section shows the different analog and digital parts which are implemented on chip.

3.1 Charge Sensitive Preamplifier

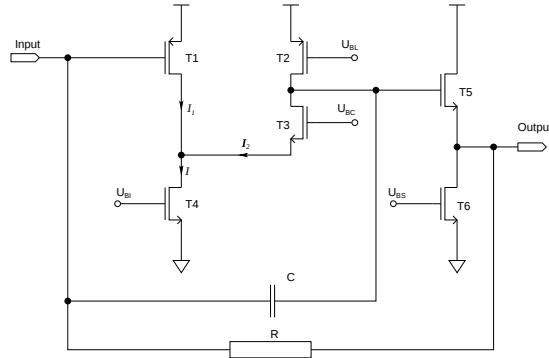


Figure 3. The preamplifier stage based on a folded cascode circuit and a source follower. The charge will be collected over the capacitance C and discharged over the resistance R .

The front-end amplifier design presented in figure 3 based on a single ended folded cascode circuit as it is frequently described in literature [3] and [6].

The main focus during the development of the charge sensitive preamplifier is on the input stage. The free circuit parameters of the input stage have to be optimized for a large detector

capacitance, the 350 kHz event rate and a low noise performance. Because the chip operates at $T = -20^{\circ}\text{C}$ there is an additional limitation of the total power consumption due to the fact of cooling capabilities.

For the used folded cascode circuit the dominant noise source is the input transistor. To reduce the noise of the input transistor a large transconductance g_m with a current biasing of 2 mA was chosen. The capacitance C is given by the maximum input charge the preamplifier has to deal with. The choice of the feedback resistor is a tradeoff between low parallel noise (large R) and the hit rate the preamplifier has to cope with (small R).

3.2 The Shaper and Output Stage

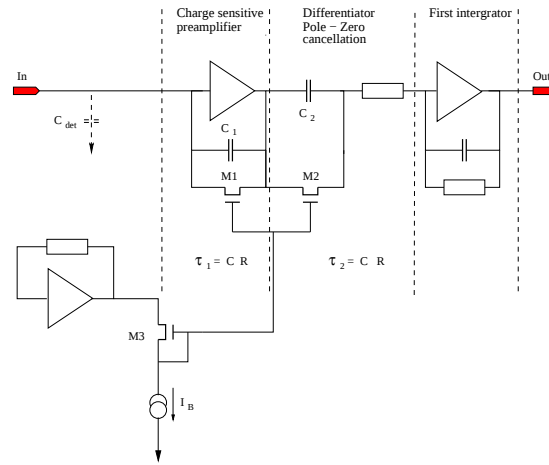


Figure 4. Shown is the charge sensitive amplifier and the first shaper stage. As feedback resistor a transistor was used. Concerning the temperature and process independency a self biasing was chosen.

To realize the mandatory high resistivity for the feedback resistor R_1 a transistor operating in the sub threshold region is used. Concerning the temperature and process independency a self biasing technic as described by O'Connor et al. in [6] is realized. To generate the gate-source voltage (V_{gs}) of the feedback transistor M1 a MOS transistor in diode connection (M3) is used together with a current sink as shown in figure 4. The source potential of this MOS diode is fixed by a downscaled version of the preamplifier circuit to guarantee the same source potential for M1, M2 and M3. The used variation of the classical pole-zero-cancellation and the scaling of M2 is described in detail in [6].

The following first integrator stage is based on a downscaled version of the preamplifier circuit which fits well to the input potential. After the first integrator stage the signal path is splitted into two subpaths as it is shown in the ASIC block diagram in figure 5. One of these subpaths has an amplification of 32 in comparison to the other to get larger output signals in the low energy range which are less sensitive to interferences by pick up noise outside the ASIC.

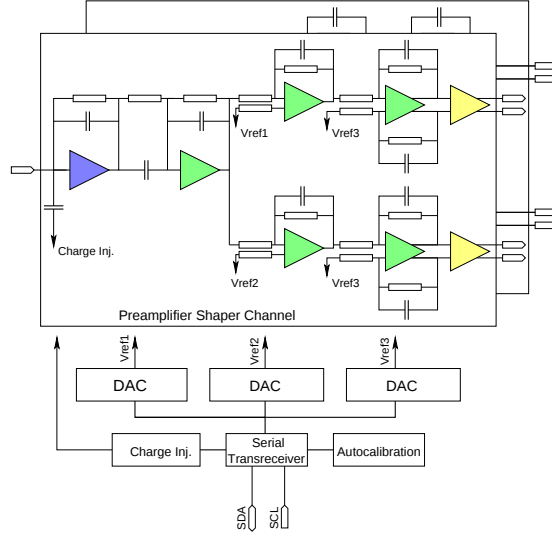


Figure 5. The readout concept of the ASIC consists of an analog readout chain and a digital part. The digital part allows to set different reference voltages to operate in a wide temperature range with the full dynamic range.

Each subpath is built up by two first order integrators. The second integrator provides a differential output signal. The following output buffers are designed to drive a load up to $20 \text{ pF} \parallel 50 \text{ k}\Omega$. The rest potentials of the second and the third integrator stage are set by three reference voltages V_{ref1} , V_{ref2} and V_{ref3} which are generated in programmable reference circuits as described later on. The APFEL - ASIC contains two identical analog channels as each crystal will be equipped with two APDs.

3.3 Digital Part

A consequence of the high amplification in the analog chain is a high temperature dependency on the output DC voltages and a change of the operating points of the amplifiers. The DC voltage dependency was measured to 25 mV/K . So with fixed voltage references a temperature shift would lead into a decreasing dynamic range of 2 %/K . To solve this adjustable voltage references are implemented.

As voltage references three 10 Bit DACs are used. To get the right DAC settings for a given temperature an autocalibration unit is attached on chip. The autocalibration process is divided into three steps. In the first step the reference voltage V_{ref1} in figure 5 is ramped until the output voltage of the second shaper stage reaches the foreseen level. Afterwards the same process is repeated with the reference voltage V_{ref2} and the output voltage of the second shaper in the low amplification path. To complete the autocalibration process in the third step the voltage reference V_{ref3} is ramped until the DC level of the shaper output comes up to the aimed value. V_{ref3} once set used by both amplification subpaths.

For monitoring purposes of the electronics a testpulser is implemented which permit a charge injection at the input of the preamplifier. A serial interface allows to write and read the DAC

settings and to trigger the autocalibration process or the testpulser. The on chip serial interface can be addressed by an individual 8 bit chip ID so a common bus structure of up to 255 ASICs can be realized. One address code is reserved for broadcast communication.

4. Measured Results

To measure the noise over a wide temperature range from $T = -30^\circ\text{C}$ to $T = +30^\circ\text{C}$ a special test setup was built. There for the ASIC is bonded on a test-PCB which is placed on a copper block cooled by a Peltier element. To avoid condensation of air humidity the whole setup is placed in an evacuated surrounding. The noise measurements for different temperatures and detector capacitances are plotted in figure 6. The equivalent input noise charge increases with a higher detector capacitance C_{Det} . Theory predicts a linear dependency which actual is observable above $C_{Det} = 100\text{ pF}$. Deviations from this linear behavior at low capacitances might result from contributions of external components.

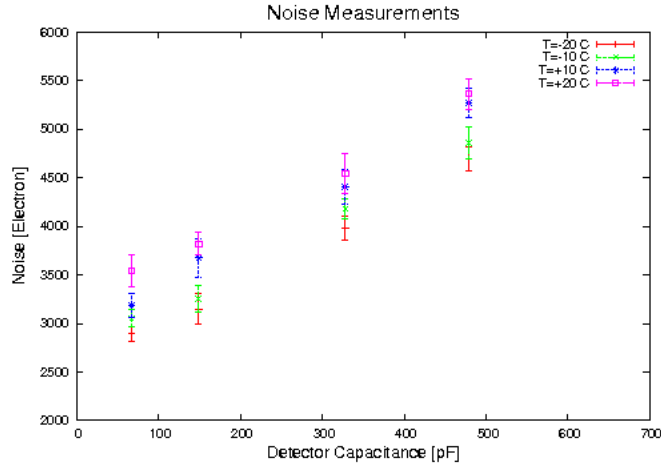


Figure 6. Results of the noise measurements for different detector capacitances and different temperatures for one readout channel.

The linear region behavior of the measured data can be described by

$$ENC_T = 2592e^- + 4.36 \frac{e^-}{\text{pF}} C_{det} + 15.9 \frac{e^-}{\text{K}} (T_K - 252\text{K}). \quad (4.1)$$

At a foreseen operating temperature of $T = -20^\circ\text{C}$ and a detector capacitance of $C_{det} = 300\text{ pF}$ an equivalent input noise charge of $ENC = 3906 e^-$ (0.62 fC) was measured which fulfills the given PANDA requirements. Figure 7 shows the results of the linearity measurements. In the plot the output amplitude as a function of the input charge is shown.

One clearly can see the linear behavior over a dynamic range of 4 orders of magnitude. The lower limit of the dynamic range is given by the previously measured noise. The upper limit is determined according to the one - dB - compression point definition for power amplifiers to a charge of 6.3 pC. This leads to a dynamic range of 10052. The preamplifier and shaper ASIC has a single supply voltage of 3.3 V. The power consumption is temperature dependent and can be described by

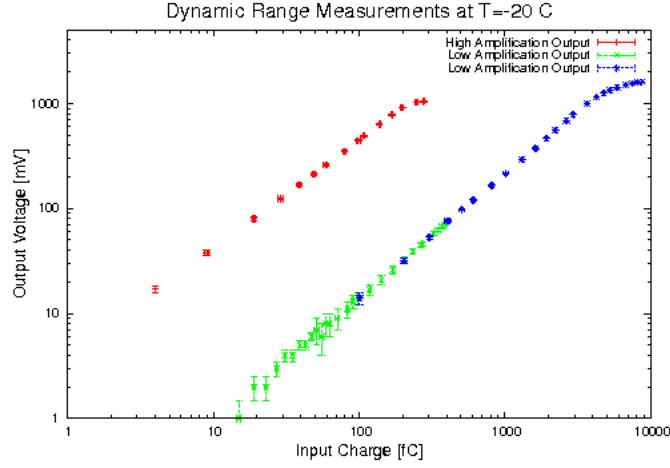


Figure 7. Results of the linearity measurements for the high and low amplification outputs of one readout channels.

$$P = 56.4 \text{ mW} - 0.124 \frac{\text{mW}}{\text{K}} (T_K - 252 \text{ K}). \quad (4.2)$$

5. Summary

In table 2 a summary of the measured results is presented. The APFEL - ASIC produced in 350 nm CMOS technology by AMS fulfills all specifications required for the PANDA EMC. Especially the results for the equivalent noise charge are distinguished as well as the large dynamic range.

Gain of		
signal path 1:	10.41 ± 0.069	mV/fC
signal path 2:	0.332 ± 0.055	mV/fC
Peaking time:	248 ± 3	ns
ENC:	0.62 ± 0.03	fC
Max. input charge:	6.31	pC
Dynamic range:	10 052	1
Power consumption:	56.5 ± 0.5	mW/Channel

Table 2. Summary of the measurement results at T=-20°C.

Acknowledgments

The authors wish to thanks the GSI experiment electronics group (EE) especially the PCB - layout group for their excellent technical and mechanical support. Our special thanks is addressed to

Harald Deppe (Gesellschaft für Schwerionenforschung) and Sven Löchner (Gesellschaft für Schwerionenforschung) for their support.

References

- [1] PANDA Collaboration, Technical Progress Report, Strong Interaction Studies with Antiprotons, February 2005
- [2] PANDA Collaboration, Design Report, Strong Interaction Studies with Antiprotons, October 2008
- [3] Chang, Z.Y., Low Noise Wide-Band Amplifiers in bipolar and CMOS technologies, Kluwer academic publishers 1991.
- [4] Laker, K.R., Sansen, W.M.C., Design of Analog integrated circuits and systems, McGraw Hill 1994.
- [5] Binkley, D.M. et al.: A low Noise, Wideband, Integrated CMOS Transimpedance Preamplifier for Photodiode Application, IEEE Trans. Nucl. Sci. Vol.39 No.4 1992 pp 747-752.
- [6] Gramegna, G., O'Connor, P., Rehak, P., Hart, S.: CMOS preamplifier for low capacitance detectors, NIM A 390 (1997) 241-250.